CLAIMS

What is claimed is:

1. A non-volatile memory cell comprising:

a latch circuit which comprises a first node and a second node and latches complementary data set in the first node and second node;

a first switching element which connects the first node to a first data input/output line;

a second switching element which connects the second node to a second data input/output line;

a first ferroelectric capacitor which connects the second data input/output line to the first node; and

a second ferroelectric capacitor which connects the first data input/output line to the second node.

2. A non-volatile memory cell according to claim 1,

in which the latch circuit comprises a first inverter and a second inverter;

the first inverter comprising a first transistor and a second transistor which complement each other and are serially connected between a power line and ground;

the second inverter comprising a third transistor and a fourth transistor which complement each other and are serially connected between the power line

and ground;

the first and second transistors each having a gate and a drain, the gates of the first and second transistors being connected to the first node and the drains of the first and second transistors being connected to the second node; and

the third and fourth transistors each having a gate and a drain, the gates of the third and fourth transistors being connected to the second node and the drains of the third and fourth transistors being connected to the first node.

3. A non-volatile memory cell according to claim 1,

in which the latch circuit comprises a third inverter and fourth inverter;

the third inverter comprising a first resistor and a fifth transistor which are serially connected between a power line and ground;

the fourth inverter comprising a second resistor and a sixth transistor which are serially connected between the power line and ground;

a gate of the fifth transistor being connected to the first node;

a source of the fifth transistor being connected to the second node;

a gate of the sixth transistor being connected to the second node;

a source of the sixth transistor being connected to the first node;

the resistance value of the first resistor being higher than the ON-resistance value of the fifth transistor; and

the resistance value of the second resistor being higher than the ON-resistance value of the sixth transistor.

4. A method of controlling a non-volatile memory cell comprising:

a latch circuit which comprises a first node and a second node and latches complementary data set in the first node and the second node;

a first switching element which connects the first node to a first data input/output line;

a second switching element which connects the second node to a second data input/output line;

a first ferroelectric capacitor which connects the second data input/output line to the first node; and

a second ferroelectric capacitor which connects the first data input/output line and the second node;

the method comprising a STORE step and a RECALL

step;

the STORE step comprising setting the potential of one of the first and second data input/output lines to a high level, setting the potential of the other data input/output line to a low level and turning on the first and second switching elements;

the RECALL step comprising a first substep and a second substep;

the first substep comprising setting the potential of a power line of the latch circuit to a ground potential, setting the potentials of the first and second data input/output lines to the ground potential and turning on the first and second switching elements;

the second substep, which follows the first substep, comprising, in the state that the potentials of the first and second data input/ output lines are maintained at the ground potential, turning off the first and second switching elements and increasing the potential of the power line of the latch circuit.

5. A method of controlling a non-volatile memory cell according to claim 4, in which the STORE step further comprises:

setting the potential of the power line of the latch circuit to the ground potential, turning on the

first and second switching elements, setting the potentials of the first and second data input/output lines to the ground potential and removing power to the non-volatile memory cell.

6. A non-volatile memory cell comprising:

a latch circuit which comprises a first node and a second node and latches complementary data set in the first node and the second node;

a first switching element which connects the first node to a first data input/output line;

a second switching element which connects the second node to a second data input/output line;

a first ferroelectric capacitor and a second ferroelectric capacitor select element which are serially connected between the second data input/output line and the first node; and

a second ferroelectric capacitor and a first ferroelectric capacitor select element which are serially connected between the first data input/output line and the second node;

the first ferroelectric capacitor being connected to the first node; and

the second ferroelectric capacitor being connected to the second node.

7. A non-volatile memory cell according to claim 6,

in which the latch circuit comprises a first inverter and a second inverter;

the first inverter comprising a first transistor and a second transistor which complement each other and are serially connected between a power line and ground;

the second inverter comprising a third transistor and fourth transistor which complement each other and are serially connected between the power line and ground;

the first and second transistors each having a gate and a drain, the gates of the first and second transistors being connected to the first node and the drains of the first and second transistors being connected to the second node; and

the third and fourth transistors each having a gate and a drain, the gates of the third and fourth transistors being connected to the second node and the drains of the third and fourth transistors being connected to the first node.

8. A non-volatile memory cell according to claim 6,

in which the latch circuit comprises a third inverter and a fourth inverter;

the third inverter comprising a first resistor and a fifth transistor which are serially connected between a power line and ground;

the fourth inverter comprising a second resistor and a sixth transistor which are serially connected between the power line and ground;

a gate of the fifth transistor being connected to the first node;

a source of the fifth transistor being connected to the second node;

a gate of the sixth transistor being connected to the second node;

a source of the sixth transistor being connected to the first node;

the resistance value of the first resistor being higher than the ON-resistance value of the fifth transistor; and

the resistance value of the second resistor being higher than the ON-resistance value of the sixth transistor.

9. A method of controlling a non-volatile memory cell comprising:

a latch circuit which comprises a first node and a second node and latches complementary data set in the

first and second nodes;

a first switching element which connects the first node to a first data input/output line;

a second switching element which connects the second node to a second data input/output line;

a first ferroelectric capacitor and a second ferroelectric capacitor select element which are serially connected between the second data input/output line and the first node; and

a second ferroelectric capacitor and a first ferroelectric capacitor select element which are serially connected between the first data input/output line and the second node;

the first ferroelectric capacitor being connected to the first node; and

the second ferroelectric capacitor being connected to the second node;

the method comprising a WRITE step, a READ step, a STORE step and a RECALL step;

the WRITE step comprising turning off the first and second ferroelectric capacitor select elements; setting the potential of one of the first and second data input/output lines to a high level and the potential of the other data input/output line to a low level, turning on the first and second switching elements, and setting

the potentials of the first and second nodes to those of the first and second data input/output lines respectively;

the READ step comprising turning off the first and second ferroelectric capacitor select elements, turning on the first and second switching elements, and setting the potentials of the first and second data input/output lines to those of the first and second nodes respectively;

the STORE step comprising, in the state that complementary data are latched into the latch circuit, turning on the first and second ferroelectric capacitor select elements and the first and second switching elements;

the RECALL step comprising a first substep and a second substep;

the first substep comprising setting the potential of a power line of the latch circuit to the ground potential, setting the potentials of the first and second data input/output lines to the ground potential, and turning on the first and second switching elements and the first and second ferroelectric capacitor select elements; and

the second substep, which follows the first substep, comprising, in the state that the first and second ferroelectric capacitor select elements are

maintained in the ON state and the potentials of the first and second data input/output lines are maintained at the ground potential, turning off the first and second switching elements and increasing the potential of the power line of the latch circuit.

10. A method of controlling a non-volatile memory cell according to claim 9,

in which the STORE step further comprises setting the potential of the power line of the latch circuit to the ground potential, turning on the first and second switching elements and the first and second ferroelectric capacitor select elements, setting the potentials of the first and second data input/output lines to the ground potential and removing power to the non-volatile memory cell.

11. A method of controlling a non-volatile memory cell comprising:

a latch circuit which comprises a first node and a second node and latches complementary data set in the first and second nodes;

a first switching element which connects the first node to a first data input/output line;

a second switching element which connects the

second node to a second data input/output line;

a first ferroelectric capacitor and a second ferroelectric capacitor select element which are serially connected between the second data input/output line and the first node; and

a second ferroelectric capacitor and a first ferroelectric capacitor select element which are serially connected between the first data input/output line and the second node;

the first ferroelectric capacitor being connected to the first node; and

the second ferroelectric capacitor being connected to the second node;

the method comprising a WRITE step, a READ step, a STORE step and a RECALL step;

the WRITE step comprising turning off the first and second ferroelectric capacitor select elements; setting the potential of one of the first and second data input/output lines to a high level and the potential of the other data input/output line to a low level, turning on the first and second switching elements, and setting the potentials of the first and second nodes to those of the first and second data input/output lines respectively;

the READ step comprising turning off the first and second ferroelectric capacitor select elements,

turning on the first and second switching elements, and setting the potentials of the first and second data input/output lines to those of the first and second nodes respectively;

the STORE step comprising setting the potential of one of the first and second data input/output lines to a high level and setting the potential of the other data input/output line to a low level, according to the complementary data latched into the latch circuit, and turning on the first and second ferroelectric capacitor select elements;

the RECALL step comprising a first substep and a second substep;

the first substep comprising setting the potential of a power line of the latch circuit to the ground potential, setting the potentials of the first and second data input/output lines to the ground potential and turning on the first and second switching elements and the first and second ferroelectric capacitor select elements; and

the second substep, which follows the first substep, comprising, in the state that the first and second ferroelectric capacitor select elements are maintained in the ON state and the potentials of the first and second data input/output lines are maintained at the

ground potential, turning off the first and second switching elements and increasing the potential of the power line of the latch circuit.

12. A method of controlling a non-volatile memory cell according to claim 11, in which the STORE step further comprises:

setting the potential of the power line of the latch circuit to the ground potential, turning on the first and second switching elements and the first and second ferroelectric capacitor select elements, setting the potentials of the first and second data input/output lines to the ground potential and removing power to the non-volatile memory cell.

13. A non-volatile memory cell comprising:

a latch circuit which comprises a first node and a second node and latches complementary data set in the first and second nodes;

a first switching element and a first control element which are serially connected between the first node and a first data input/output line;

a second switching element and a second control element which are serially connected between the second node and a second data input/output line;

a second ferroelectric capacitor and a first ferroelectric capacitor select element which are serially connected between the second node and a third node, the third node serially connecting the first switching element and the first control element; and

a first ferroelectric capacitor and a second ferroelectric capacitor select element which are serially connected between the first node and a fourth node, the fourth node serially connecting the second switching element and the second control element;

the first switching element being connected to the first node;

the second switching element being connected to the second node;

the first ferroelectric capacitor being connected to the first node; and

the second ferroelectric capacitor being connected to the second node.

14. A non-volatile memory cell according to claim 13,

in which the latch circuit comprises a first inverter and a second inverter,

the first inverter comprising a first transistor and a second transistor which complement each other and are serially connected between a power line and ground;

the second inverter comprising a third transistor and a fourth transistor which complement each other and are serially connected between the power line and ground;

the first and second transistors each having a gate and a drain, the gates of the first and second transistors being connected to the first node and the drains of the first and second transistors being connected to the second node;

the third and fourth transistors each having a gate and a drain, the gates of the third and fourth transistors being connected to the second node and the drains of the third and fourth transistors being connected to the first node.

15. A non-volatile memory cell according to claim 13,

in which the latch circuit comprises a third inverter and a fourth inverter;

the third inverter comprising a first resistor and a fifth transistor which are serially connected between a power line and ground;

the fourth inverter comprising a second resistor and a sixth transistor which are serially connected between the power line and ground;

a gate of the fifth transistor being connected

to the first node;

a source of the fifth transistor being connected to the second node;

a gate of the sixth transistor being connected to the second node;

a source of the sixth transistor being connected to the first node;

the resistance value of the first resistor being higher than the ON-resistance value of the fifth transistor; and

the resistance value of the second resistor being higher than the ON-resistance value of the sixth transistor.

16. A method of controlling a non-volatile memory cell comprising:

a latch circuit which comprises a first node and a second node and latches complementary data set in the first and second nodes;

a first switching element and a first control element which are serially connected between the first node and a first data input/output line;

a second switching element and a second control element which are serially connected between the second node and a second data input/output line;

a second ferroelectric capacitor and a first ferroelectric capacitor select element which are serially connected between the second node and a third node, the third node serially connecting the first switching element and the first control element; and

a first ferroelectric capacitor and a second ferroelectric capacitor select element which are serially connected between the first node and a fourth node, the fourth node serially connecting the second switching element and the second control element;

the first switching element being connected to the first node;

the second switching element being connected to the second node;

the first ferroelectric capacitor being connected to the first node; and

the second ferroelectric capacitor being connected to the second node;

the method comprising a WRITE step, a READ step, a STORE step and a RECALL step;

the WRITE step comprising turning off the first and second ferroelectric capacitor select elements; setting the potential of one of the first and second data input/output lines to a high level and the potential of the other data input/output line to a low level, turning

on the first and second switching elements and the first and second control elements, and setting the potentials of the first and second nodes to those of the first and second data input/output lines respectively;

the READ step comprising turning off the first and second ferroelectric capacitor select elements; turning on the first and second switching elements and the first and second control elements, and setting the potentials of the first and second data input/output lines to those of the first and second nodes respectively;

the STORE step comprising setting the potential of one of the first and second data input/output lines to a high level and the potential of the other data input/output line to a low level, according to the complementary data latched into the latch circuit, and turning on the first and second control elements and the first and second ferroelectric capacitor select elements;

the RECALL step comprising a first substep and a second substep;

the first substep comprising setting the potential of a power line of the latch circuit to the ground potential, setting the potentials of the first and second data input/output lines to the ground potential, and turning on the first and second switching elements, the first and second ferroelectric capacitor select

elements and the first and second control elements;

the second substep, which follows the first substep, comprising, in the state that the first and second ferroelectric capacitor select elements and the first and second control elements are maintained in the ON state and the potentials of the first and second data input/output lines are maintained at the ground potential, turning off the first and second switching elements and increasing the potential of the power line of the latch circuit.

17. A method of controlling a non-volatile memory cell according to claim 16, in which the STORE step further comprises:

setting the potential of the power line of the latch circuit to the ground potential, turning on the first and second switching elements, the first and second ferroelectric capacitor select elements and the first and second control elements, setting the potentials of the first and second data input/output lines to the ground potential and removing power to the non-volatile memory cell.

18. A method of controlling a non-volatile memory cell comprising:

a latch circuit which comprises a first node and a second node and latches complementary data set in the first and second nodes;

a first switching element and a first control element which are serially connected between the first node and a first data input/output line;

a second switching element and a second control element which are serially connected between the second node and a second data input/output line;

a second ferroelectric capacitor and a first ferroelectric capacitor select element which are serially connected between the second node and a third node, the third node serially connecting the first switching element and the first control element; and

a first ferroelectric capacitor and a second ferroelectric capacitor select element which are serially connected between the first node and a fourth node, the fourth node serially connecting the second switching element and the second control element;

the first switching element being connected to the first node;

the second switching element being connected to the second node;

the first ferroelectric capacitor being connected to the first node; and

the second ferroelectric capacitor being connected to the second node;

the method comprising a WRITE step, a READ step, a STORE step and a RECALL step;

the WRITE step comprising turning off the first and second ferroelectric capacitor select elements, setting the potential of one of the first and second data input/output lines to a high level and the potential of the other data input/output line to a low level, turning on the first and second switching elements and the first and second control elements, and setting the potentials of the first and second nodes to those of the first and second data input/output lines respectively;

the READ step comprising turning off the first and second ferroelectric capacitor select elements, turning on the first and second switching elements and the first and second control elements, and setting the potentials of the first and second data input/output lines to those of the first and second nodes respectively;

the STORE step comprising, in the state that complementary data are latched into the latch circuit; turning off the first and second control elements and turning on the first and second switching elements and the first and second ferroelectric capacitor select elements;

the RECALL step comprising a first substep and a

second substep;

the first substep comprising setting the potential of a power line of the latch circuit to the ground potential, setting the potentials of the first and second data input/output lines to the ground potential, and turning on the first and second switching elements, the first and second ferroelectric capacitor select elements and the first and second control elements;

the second substep, which follows the first substep, comprising, in the state that the first and second ferroelectric capacitor select elements and the first and second control elements are maintained in the ON state and the potentials of the first and second data input/output lines are maintained at the ground potential, turning off the first and second switching elements and increasing the potential of the power line of the latch circuit.

19. A method of controlling a non-volatile memory cell according to claim 18,

in which the STORE step further comprises setting the potential of the power line of the latch circuit to the ground potential, turning on the first and second switching elements, the first and second ferroelectric capacitor select elements and the first and

second control elements, setting the potentials of the first and second data input/output lines to the ground potential and removing power to the non-volatile memory cell.